SSPD 2015

Sensor Signal Processing for Defence Conference

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RCPE _ WiFi, password chiron1681

Advanced Signal Processing with MATLAB & Simulink

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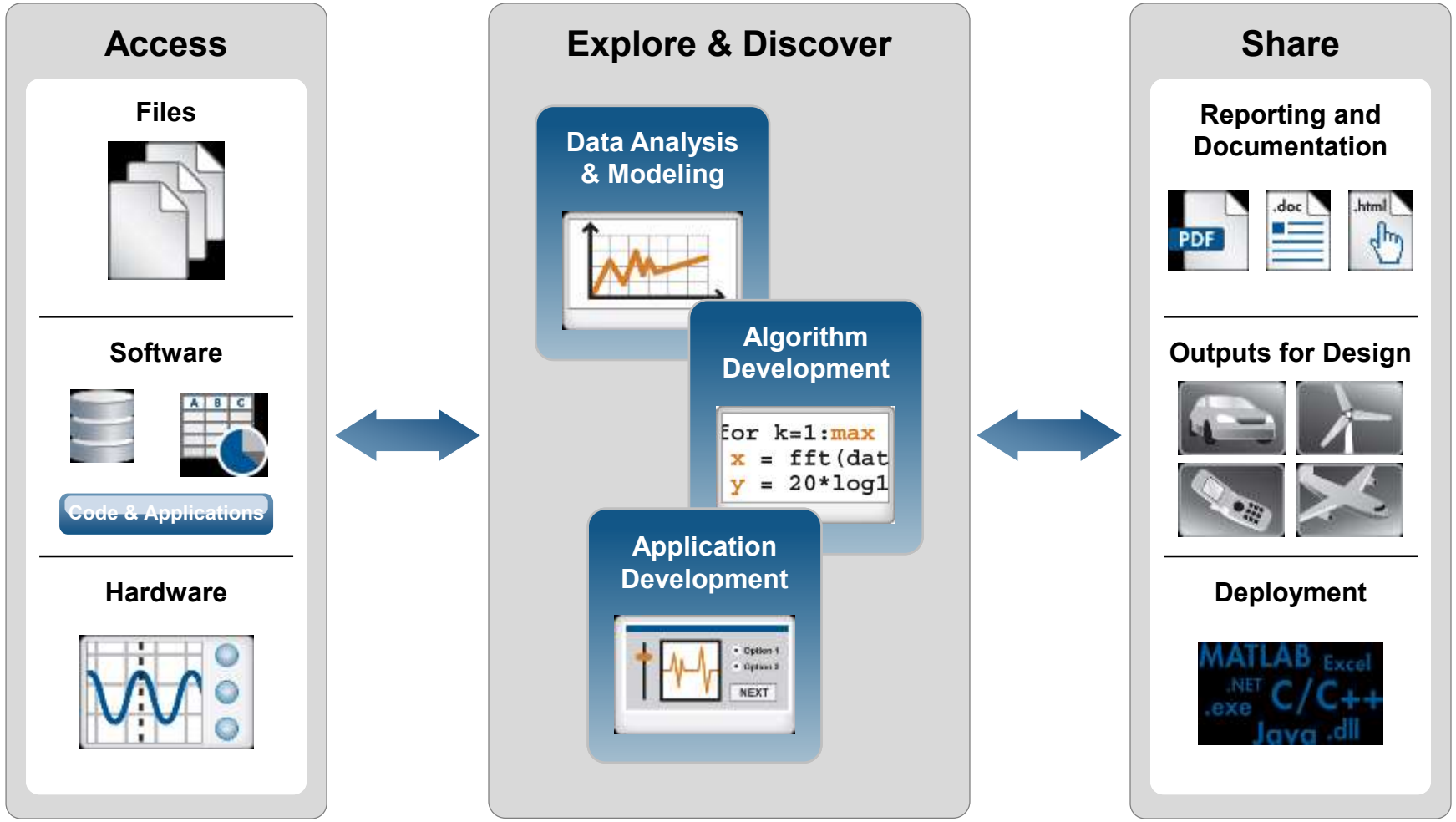
Introduction & Agenda

- A **complete workflow** for developing **advanced signal processing** systems
- **Toolboxes**: packaging proven algorithms
- **Sharing**: functions, classes, toolboxes and apps
- **Production**: HDL code generation case study

MATLAB & Simulink: Tools for a Complete Workflow

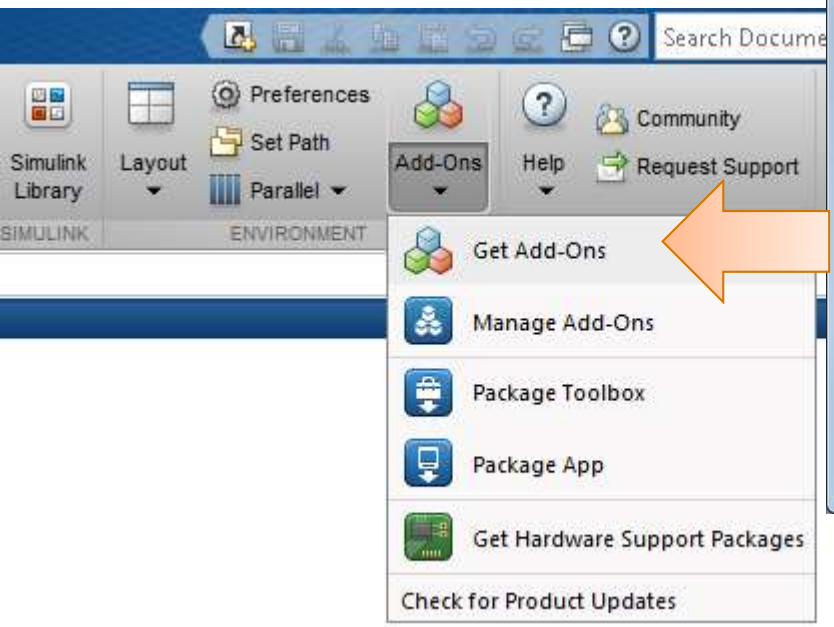


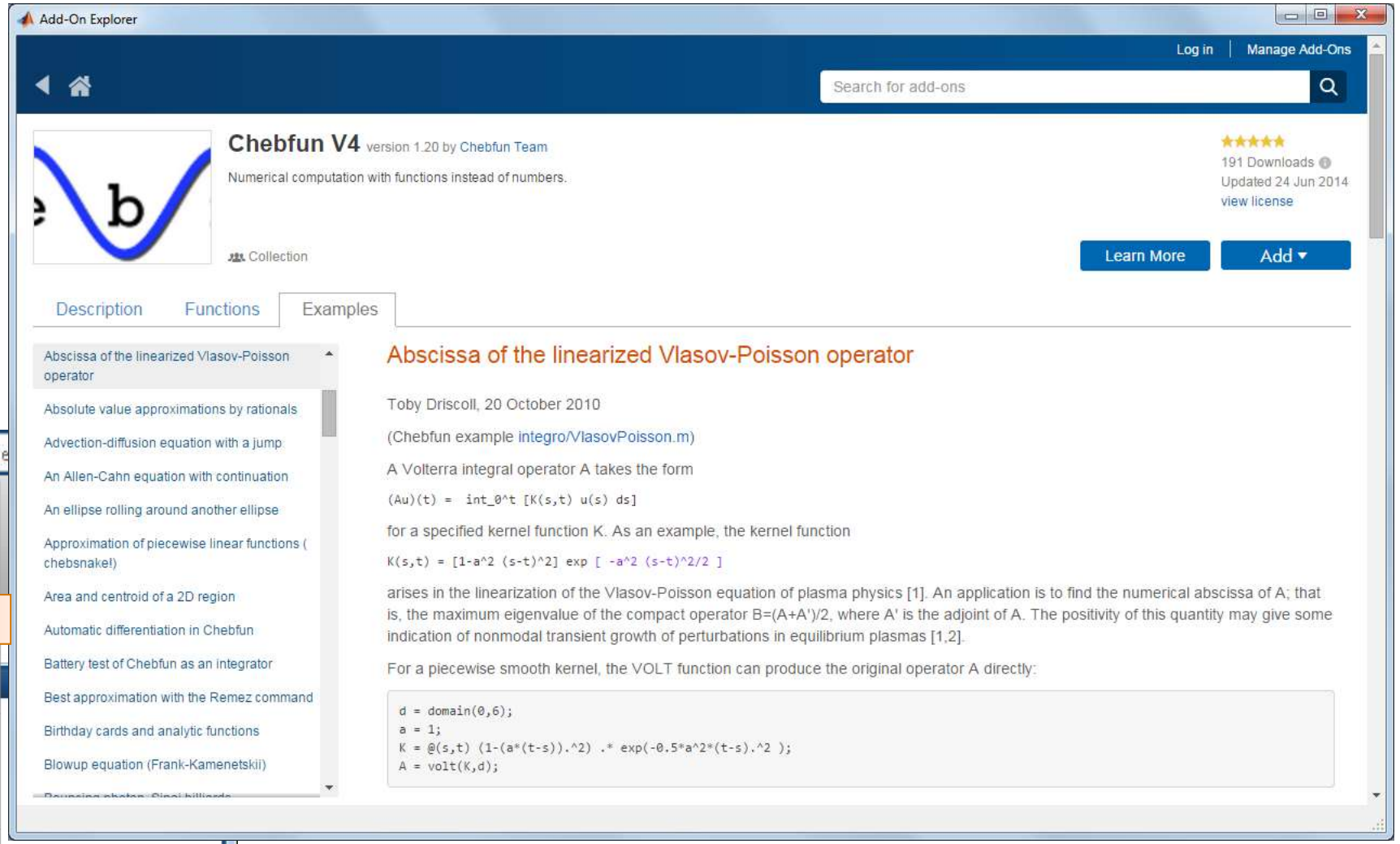
MathWorks and Advanced Signal Processing

- Toolboxes
  - Packaging of proven algorithms as demanded by the field
  - Building blocks for advanced signal processing systems
- Simulation Technology
  - High performance execution of algorithms
  - Multi-threaded execution and GPU acceleration
- Prototyping & Deployment
  - C/C++ code generation
  - HDL code generation
  - Hardware support packages

Add-Ons: from MathWorks and the User Community

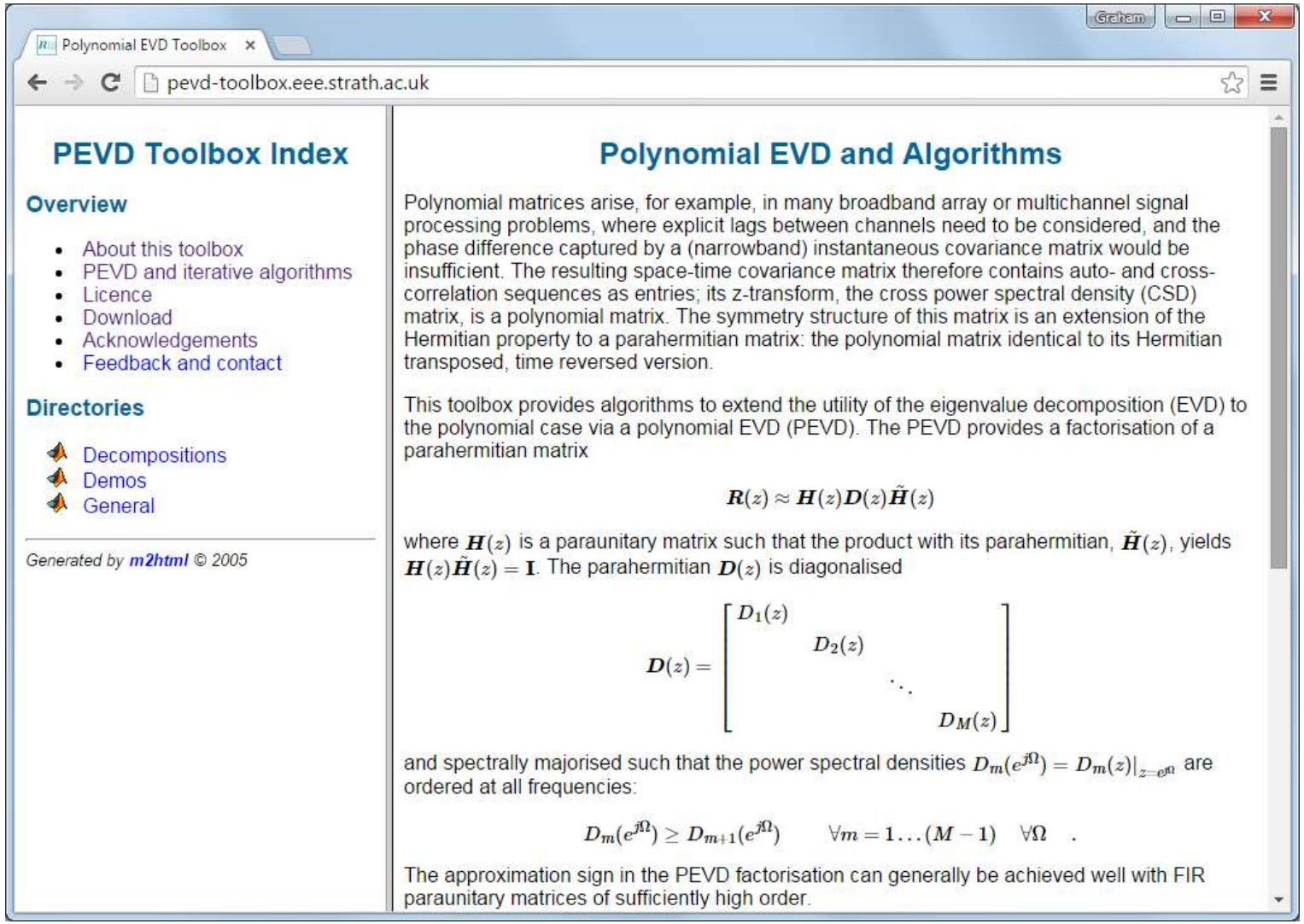
MathWorks	267
Community	19,287



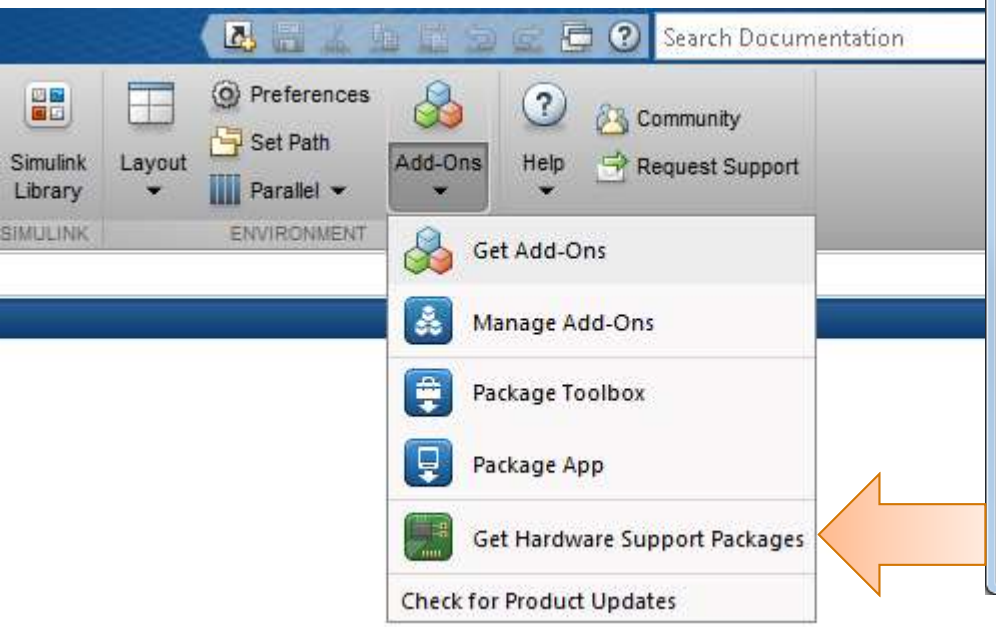


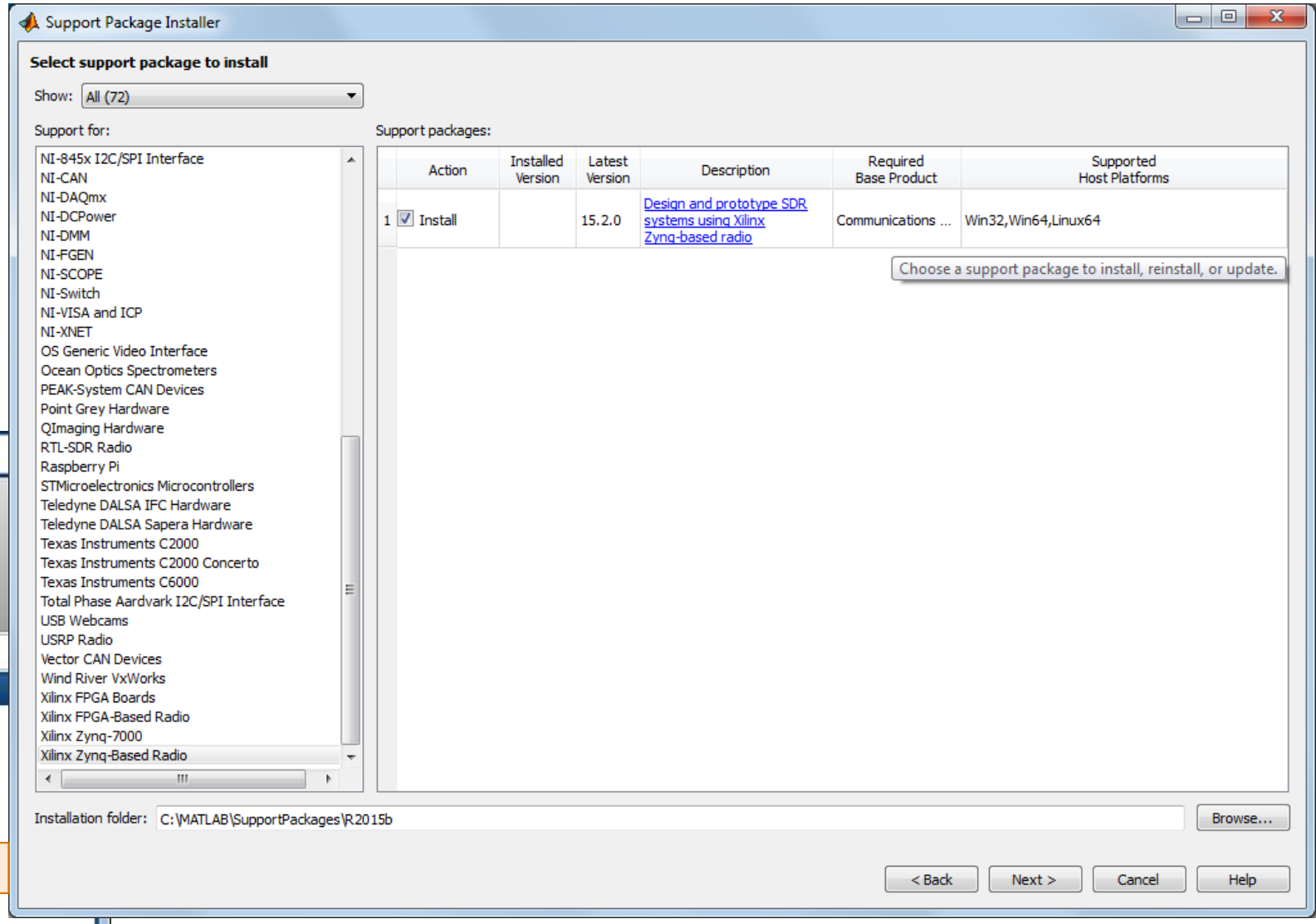
PEVD Toolbox (Polynomial Eigenvalue Decomposition)

- Available from University of Strathclyde
- Development work supported by EPSRC and the UDRC
- http://pevd-toolbox.eee.strath.ac.uk

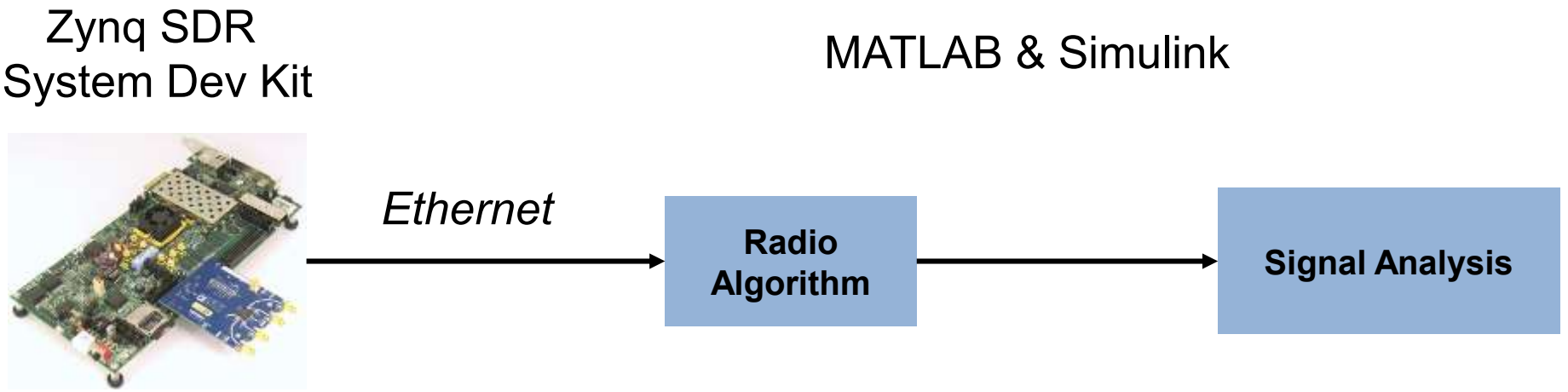


Hardware Support Packages





Radio Design Framework

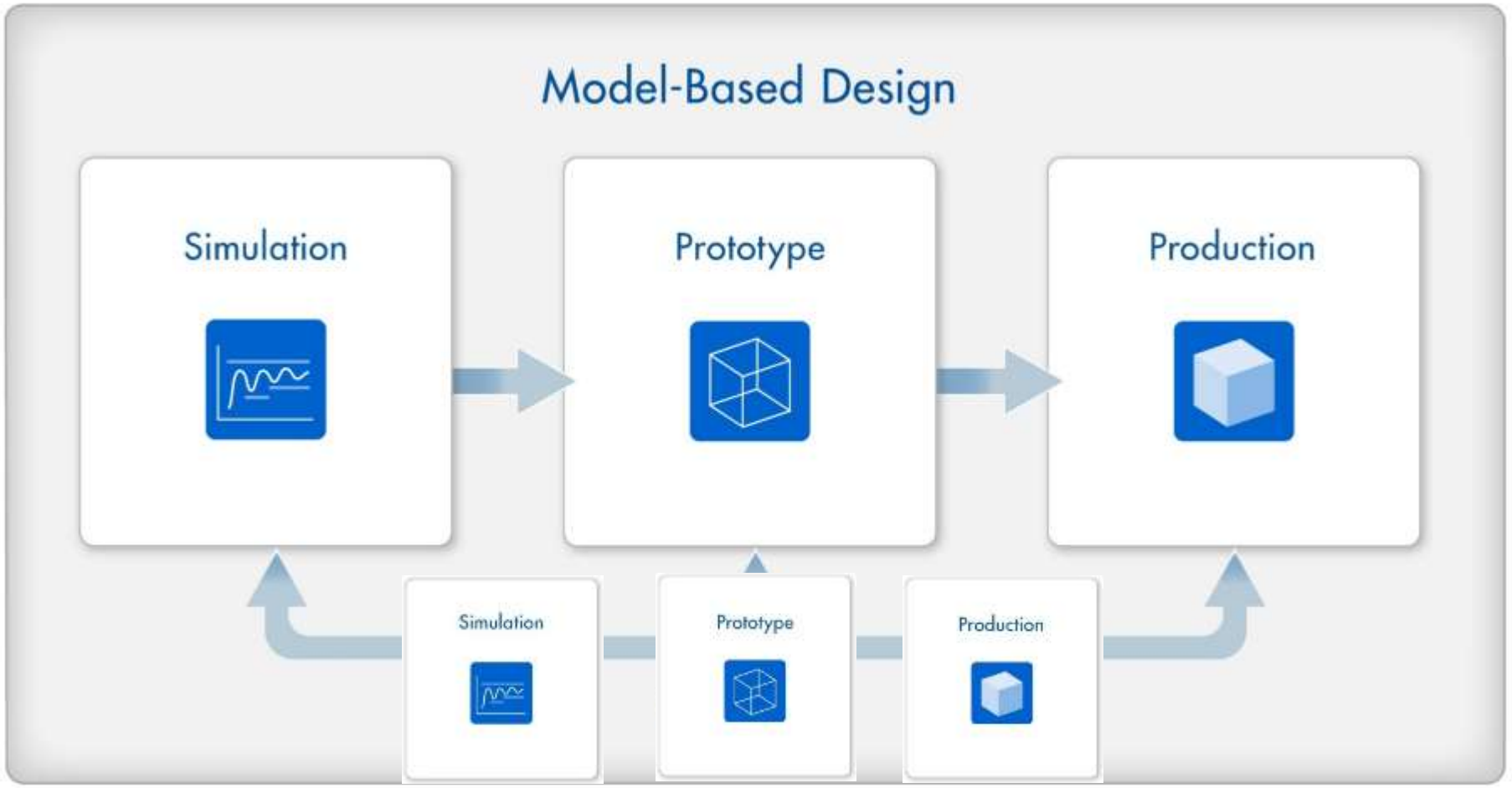


Develop and tune algorithms with off-the-air radio signals

Zynq SDR System Development Kit supports analog capture and export to Simulink

Model-Based Design

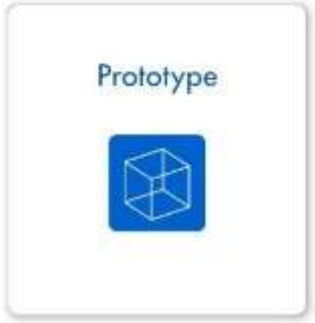
A single shared development environment



Model-Based Design

A single shared development environment

Verify algorithms and explore alternatives

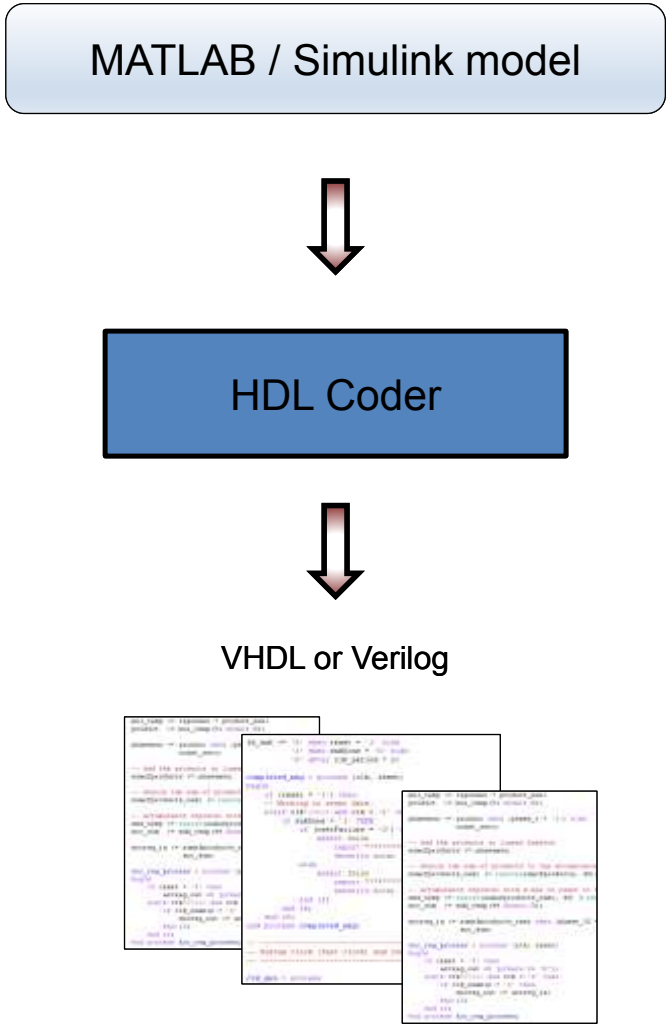


Validate performance with live data

Deploy design on production system

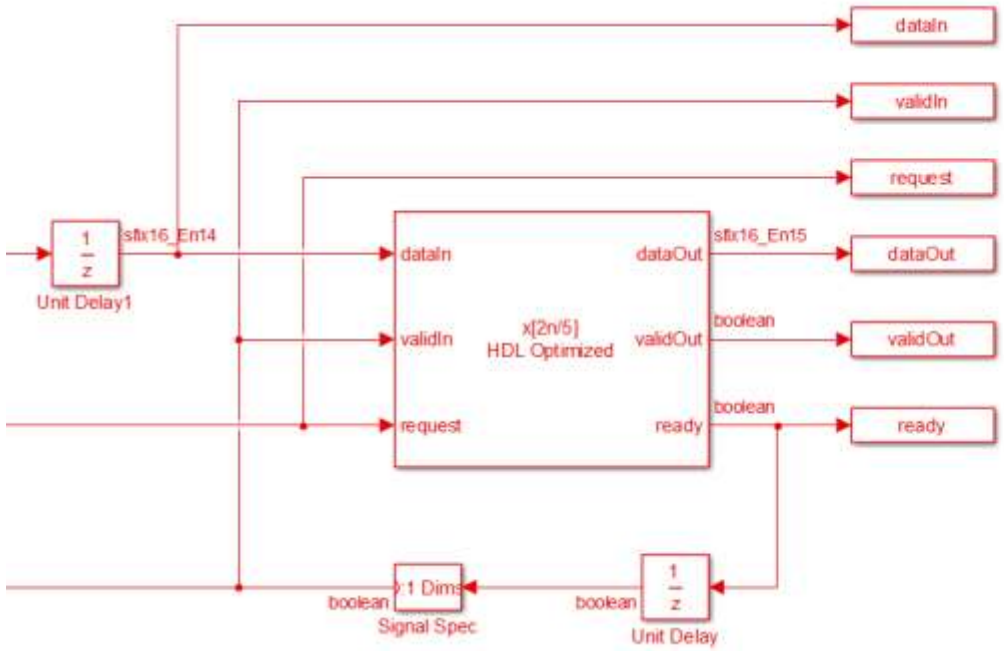
Prototyping and Deployment on FPGAs and ASICs

- HDL Coder
  - Generate synthesizable VHDL & Verilog
  - Testbench generation
  - Integration with synthesis & implementation tools
- Algorithm support
  - DSP
  - Communications
  - Vision
- A few examples . . .



HDL FIR Rate Conversion Simulink Block

- Rational factor (*L*/*M*) sample rate conversion
- Polyphase implementation
- HDL code generation + hardware friendly interface



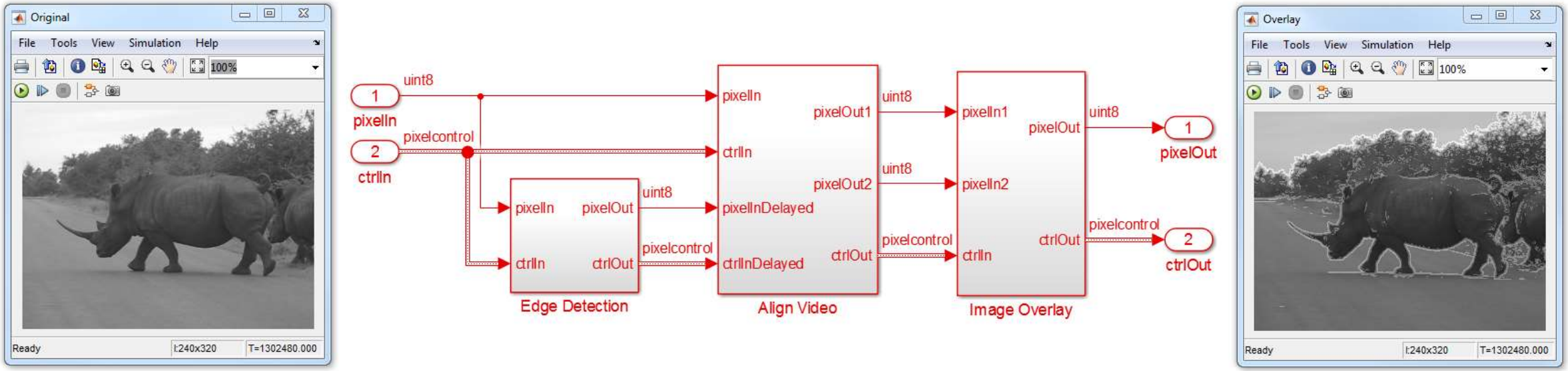
Vision HDL Toolbox – Released in R2015a

"Vision HDL Toolbox™ provides pixel-streaming algorithms for the design and implementation of vision systems on FPGAs and ASICs.

- Analysis & Enhancement
  - Edge Detection
  - Median Filter
- Conversions
  - Chroma Resampling
  - Color-Space Converter
  - Demosaic Interpolator
  - Gamma Corrector
  - Look-up Table
- Filtering
  - Image Filter
  - Median Filter
- Morphological Operations
  - Dilation, Erosion,
  - Opening, Closing
- Statistics
  - Histogram
  - Image Statistics
- I/O Interfaces
  - Frame to Pixels
  - Pixels to Frame
  - FPGA In the Loop (FIL)
- Utilities
  - Pixel Control Bus Creator
  - Pixel Control Bus Selector

Vision HDL Toolbox – Edge Detection Example

- Design framework for pixel-streaming systems
- Library of pixel-streaming algorithms
- Generate optimized HDL code



Concluding Remarks

- **Tools for a complete workflow**
- Platform for algorithm development and exploration
- High performance simulation environment
- Toolboxes which package proven algorithms
- Sharing of functions, classes, toolboxes and apps
- Production & prototyping

Thank you!

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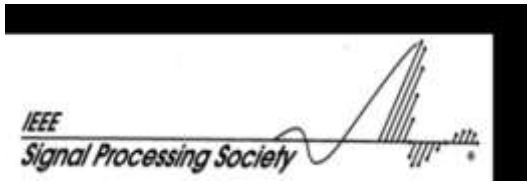

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